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STUDY OF QCA BASED DIGITAL LOGIC CIRCUITS TO BE USED IN NANOTECHNOLOGY

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ABSTRACT

Conventional CMOS has dominated manufacturing industry since last few decades but now we live in a highly sophisticated era in terms of technology so our needs of Higher speed, Reduced Area and lesser Power can not be fulfilled by traditional CMOS technology. The problem of Power Dissipation and Leakage Current can not be overcome by further Scaling of CMOS parameters. It is better to shift towards new alternatives of IC Designing. Quantum Dot Cellular Automata (QCA) based on interacting Quantum dots which is more suitable for logic circuits with superior and low power scattering at nanometer scale is possibly the best alternative among all.

In this paper one-bit magnitude comparator is made using XOR Gate and the effective area is considerably reduced compared to previous design. The Layout of AND Gate , OR Gate, NAND Gate, NOR Gate, XOR Gate, XNOR Gate, D Latch, SR Latch and JK Flip Flop is also made using QCA Technology and the comparison between the area of these gates and their previous design is shown. By utilizing this incipient nanotechnology design we can enter in an era of ultra low power.

Keywords: *QCA Designer, Majority Voter, comparator, Flip Flop.*

I. INTRODUCTION

QUANTUM DOT CELLULAR AUTOMATA is potential replacement of CMOS technology because severe effect of quantum phenomenon on the ever tinier transistor operation will not let the further miniaturization of parameters in CMOS technology. QCAs were introduced in 1993 by lent et al, and were physically verified in 1997. It can yield high device density, ultra low power consumption and high switching speed. The QCA offers a novel computing paradigm in nanotechnology. QCA structures are constructed as an array of quantum cells within which every cell has an electrostatic interaction with its neighbouring cells. QCA utilizes a new form of computation, where state of electron rather than the traditional current, contains the digital information. Instead of interconnecting wires, the cells transfer the information throughout the circuit

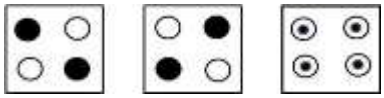
[1]. The main advantages of QCA technology are [2]

- high thickness
- very high operational recurrence
- low power utilization

Section II describes the overview of QCA technology. Implementation of QCA circuits and Simulation results of 1-bit magnitude comparator, AND, NAND, OR, NOR, XOR, XNOR Gate, D Latch, SR Latch, JK Flip Flop are discussed in Section III Conclusion and Result is in Section IV.

II. QCA OVERVIEW

The basic device in QCA is "QCA-cell" [3] which let us perform both the computation and transmission of the information through the circuit. A simple QCA cell consists of a conjectural square shaped space in which there are four energy sites in which electrons can reside. This space for electron is represented by a Dot in the cell. The dots are coupled through quantum mechanical tunnelling barriers and electrons can tunnel through them depending on the state of the system. Columbic repulsion compels the electrons to occupy the farthest dots in a cell which corresponds to the lowest energy state of the system. Cell polarization refers to the relative positions of the electrons in a cell and it decides whether it is representing binary '1' or '0'. Two types of QCA cells are there first is 90° and second is 45°cells.Figure 1. shows a 90° cells with polarization state of P = +1 which represents binary 1. The clock signal provides the needed power to perform the computation.



Polarization 1 (b) Polarization 0 (c) Null State Figure 1 QCA cell polarization

(A)QCA WIRE

QCA cells arranged in a cascaded fashion makes a QCA Wire. The attraction and repulsion occurring due to coulomb force between the adjacent cells cause the polarization of a cell so that it can align according to its neighbouring cells so the transmission of information along the array of cells occur. QCA wires transmitting binary '1' using 90° cells is shown in figure 2 here the input cell is driven by an external source and is strongly polarized in one direction. The input cell drives other cells in the NULL state which tend to align themselves to the input cell polarization to reach the system's ground state.[4].

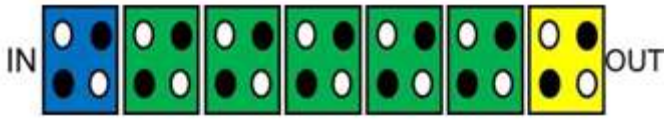


Figure 2. Transmitting binary '1' in QCA Wire

(B)MAJORITY AND & OR GATES

The structure of majority gate is shown in Figure 3. The output F is defined as F = AB+AC+BC. Output cell of the gate polarizes according to the computation cell in the center of the gate. Now this output F can be propagated with a help of QCA wire which can act as an input to other gates. The majority gate is used to build the AND and OR gates. If one of the inputs is fixed to 0/1, the resulting function F is the AND/OR of remaining two inputs[4].

Y = M(A, B,C) = AB + BC + CA

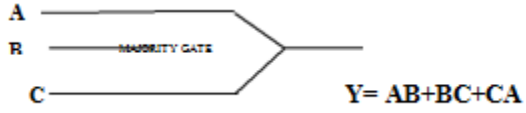


Figure 3.Majority Gate

(C) QCA CLOCKING

The information flow in QCA circuits is managed and controlled by the clock. Clocking provides the power gain and avoids the meta-stable states [5- 6]. With respect to QCA-cell the meta-stable state corresponds to polarization of a cell that cannot be distinctively identified as logic 1 or logic 0. The clock in QCA technology is not same as they are in traditional CMOS circuits, QCA clocking scheme consists of four phases: *switch* (unpolarized cells are driven by some input and get polarized depending on their neighbors' polarization), *hold* (cells are held in same binary state so that it can be used as an input to other cells), release (barriers are lowered and cells become

unpolarized) and Relax(cells remain unpolarized) [7-8]. There is a phase difference of quarter cycle in all these clocking phases which can be implemented by generating four clocks each with π/2 phase difference from previous one shown in figure4.

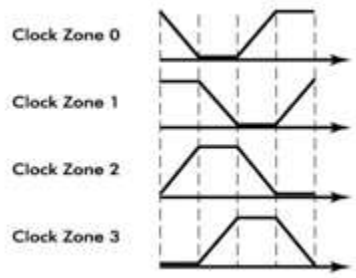


Figure 4. Four Phases of QCA Clock

(D) QCA DESIGNER

QCA Designer is a tool to simulate complicated QCA circuit layouts. First it was developed at the ATIPS Laboratory, University of Calgary, The current version of QCA Designer has three different simulation engines included. Each of the three engines has a different and important set of benefits and drawbacks. Additionally, each simulation engine can perform an exhaustive verification of the system or a set of user selected vectors. [9-10].

III. QCA IMPLEMENTATION

1. One-bit magnitude comparator

A magnitude comparator is a tool to compare two numbers which are fed at its inputs form and decides whether one number is greater than, less than or equal to the other number. Comparators are mostly in the CPU 'S and microcontrollers and thus have gained popularity and optimized in CMOS technology.[11] The proposed design of 1-bit comparator is made using a XOR Gate[12].

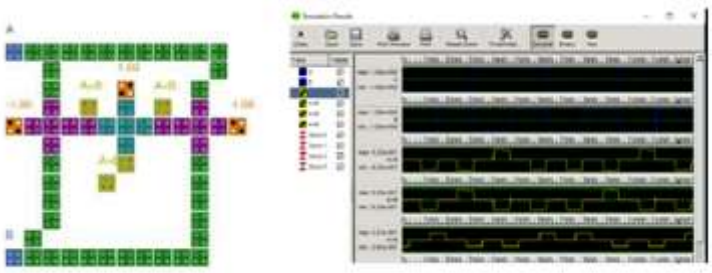


Figure 5 Layout of 1-bit magnitude comparator and its simulation Result.

Table I Comparison of cell counts

QCA Comparator	No of cells	Area in μm^2
Previous 1-bit Magnitude comparator	100	0.13 μm^2
Proposed 1-bit Magnitude comparator	61	0.08 μm^2

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2. OR Gate

The functionality of OR Gate is obtained by fixing one input of Majority Gate as '1'.

Y = AB+ BC+CA : put C=1 Y= AB+B+A
Y=A+B i.e the output of an OR Gate.

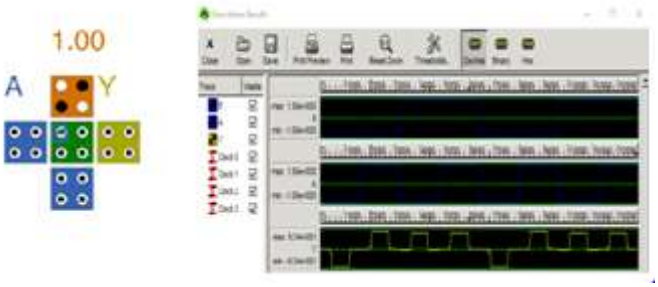

Figure 6 Layout of OR Gate [13-16] and its simulation result

3. AND Gate

The functionality of AND Gate is obtained by fixing one input of Majority Gate as '0'
Y = AB+ BC+CA put C=0
Y=AB+0+0

Y=A+B i.e the output of an AND Gate

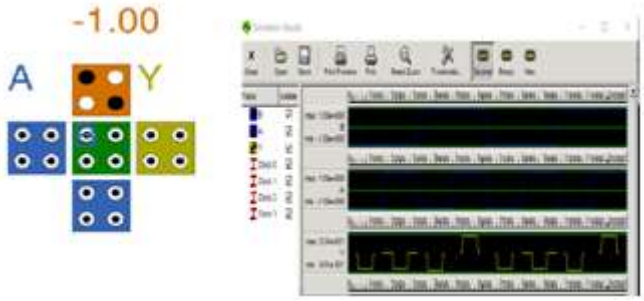

Figure 7 Layout of AND Gate[13-16] and its simulation waveform

4. .NOR and NAND Gate

To achieve the functionality of NOR Gate and NAND Gate we simply invert the output of OR and Number of cells AND Gate respectively.

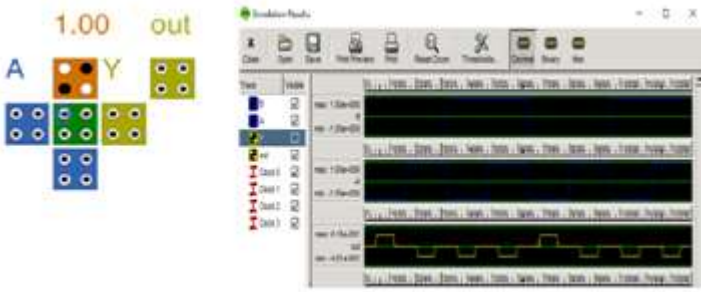

Figure 8 Layout of NOR Gate and its simulation waveform

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Figure 9 Layout of NAND Gate and its simulation waveform

5. Layout of XOR

In XOR gate output is '1'if the number of inputs are odd else is '0'. The layouts are designed with less number of cells as shown in Figure 10.

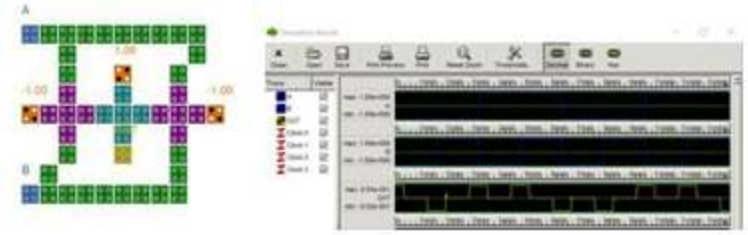

Figure 10 Layout of XOR Gate and its simulation waveform

Table II cell count comparison of XOR Gate

QCA Circuit	Number of cells	Area
Previous XOR Gate	58	0.08 μm^2
XORGatewith reduced cells	46	0.05 μm^2

6. XNOR Gate

XNOR gate act as equivalence logic and its output is '1' when both of its inputs are same. Layout is shown in figure 11.

Figure 11 Layout of XNOR Gate[17] and its simulation waveform

7. D Latch

D Latch act as a buffer. Its ouput always follows input. Figure 12 shows the Layout and simulation result of the D Latch by using QCA designer. The output is follwing the input clock pulse

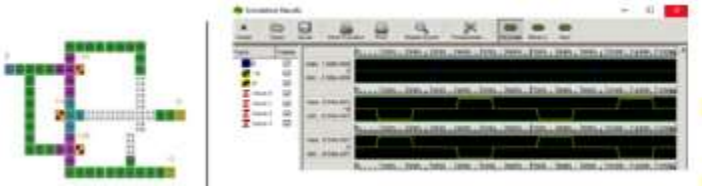

Figure 12 Layout of D Latch and its simulation waveform[18]

8. SR Latch

Figure 13 shows the QCA RS latch proposed in together with simulation results. For active high RS latch, the outputs SET when S=1 and R=0, output is RESET when R=1 and S=0.

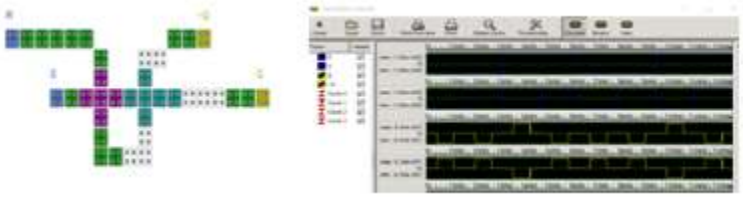

Figure 13 Layout of SR Latch and its waveform

9. JK Flip Flop

Fig.14 shows the circuits of JK flip flop and its simulation using QCA Designer. JK flip flop toggles the previous output when both of its inputs are logic 1.All other outputs of JK Flip Flop are same as that of a S R Latch.

Figure 14 Layout of JK Flip Flop

IV. RESULT AND CONCLUSION

The area of proposed 1-bit magnitude comparator has been reduced from 0.13μm^2 to 0.08 μm^2 and the cell count has been reduced from 100 cells to 61 cells .Area of XOR Gate has been reduced from 0.08 μm^2 to 0.05 μm^2 and cell count has been reduced from 58 to 46.

Number of cells in D Latch has been reduced from 73 to 68. The layout of AND, OR, NAND, NOR, XOR, XNOR. SR Latch and JK Flip Flop are made and their Simulation waveform are same as they were in reference papers so their functionality has been verified. There is a need to focus more and more on QCA so that it can be proved a potential replacement of conventional CMOS design in near future when traditional technology will no longer be able to be minimised further.

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